FIELD-EFFECT TRANSISTOR (FET) FAILURE ANALYSIS

MARVIN TARANG ANAK EDWARD SUKA

DISSERTATION SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE BACHELOR OF SCIENCE WITH HONOURS

PHYSICS WITH ELECTRONICS PROGRAM
SCHOOL OF SCIENCE AND TECHNOLOGY
UNIVERSITY MALAYSIA SABAH

April 2008

PUMS99:1

UNIVERSITI MALAYSIA SABAH

BORANG PENGESAHAN STATUS TESIS@

JUDUL: FIELD - EFFECT TRANSISTOR (FET) FAILURE ANALYSIS

IJAZAH: SARJANA MUDA SAINS DENGAN KEPUJIAN DALAM FIZIK DENGAN ELEKTRONIK.

SAYA MARVIN TARANG ANAK EDWARD SESI PENGAJIAN: 2007/2008
(HURUF BESAR)

mengaku membenarkan tesis (LPSM/Sarjana/Doktor Falsafah) ini disimpan di Perpustakaan Universiti Malaysia Sabah dengan syarat-syarat kegunaan seperti berikut:-

1. Tesis adalah hakmilik Universiti Malaysia Sabah.
2. Perpustakaan Universiti Malaysia Sabah dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan tesis ini sebagai bahan pertukaran antara institutsi pengajian tinggi.
4. Sila tandakan (/)

☐ SULIT	(Mengandungi maklumat yang berdarjah keselamatan atau Kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐ TERHAD	(Mengandungi maklumat TERHAD yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)
☒ TIDAK TERHAD	

Disahkan Oleh

NURULAIN BINTI ISMAIL
LIBRARIAN
UNIVERSITI MALAYSIA SABAH

(TANDATANGAN PENULIS)

(TANDATANGAN PUSTAKAWAN)

Alamat Tetap: LOT 10385, LRG A9, BDC STAMPIN, JLN STUTONG, 93350, KUCHING, SARAWAK.

Nama Penyelia

Tarikh: 12/5/2008

Tarikh: ___ _ ___

CATATAN:- *Potong yang tidak berkenaan.
**Jika tesis ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa /organisasi berkenaan dengan menyatakan sekali sebab dan tempoh tesis ini perlu dikelaskan sebagai SULIT dan TERHAD.
@Tesis dimaksudkan sebagai tesis bagi Ijazah Doktor Falsafah dan Sarjana secara penyelidikan atau disertai bagi pengajian secara kerja kursus dan Laporan Projek Sarjana Muda (LPSM).

DECLARATION

I declare that this dissertation is my own product except for the statement where each has been cited.

4 April 2008

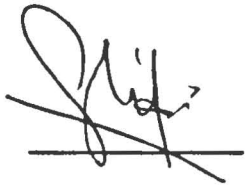
MARVIN TARANG ANAK EDWARD SUKA

HS 2004 - 4830

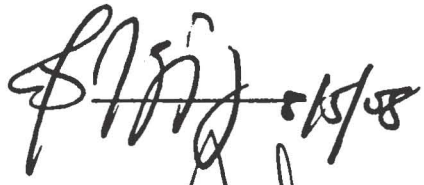
CERTIFIED BY:

Signature

1. SUPERVISOR
(MR. SAAFIE SALLEH)



2. EXAMINER 1
(PROF DR. FAUZIAH Hj. ABDUL AZIZ)



3. EXAMINER 2
(MR. ALVIE LO SIN VOI)

4. DEAN
(PROF. MADYA DR. SHARIFF A.KADIR S. OMANG)

ACKNOWLEDGEMENT

Praise is to God upon His permission I could complete this thesis. Words are hardly adequate to express my gratitude to a number of persons for their kind and generous help during the times that this study was in the making.

I take this opportunity especially to thank my supervisor, Mr. Saafie Salleh for his endless advices and tireless support for the crucial progress of this thesis.

Many thanks also go to Mr. Rahim and Mr. Nazri who are the laboratory assistants at the School of Science and Technology (SST) in University Malaysia Sabah.

I also would like to thank my Physics and Electronics course mates for their help and friendship are much appreciated.

My utmost gratitude has to go to my family for their invaluable support and motivation to finish this project.

To the many individuals whose names are not mentioned, your efforts are not forgotten and are acknowledged. Your help, even in the tiniest way, certainly has a big impact on the completion of this project.

Working on this project has been a journey of faith for me; for this experience, I thank God.

MARVIN TARANG ANAK EDWARD SUKA (HS 2004 – 4830)
4 April 2008

ABSTRACT

This research is a failure analysis of the metal-oxide semiconductor field effect transistor (MOSFET) where the change of threshold voltage value, V_{TH}, with the increase of temperature on the transistor is observed. In this research, the MPF 990 n-channel enhancement mode MOSFET is used. These transistors are first tested to confirm their good conditions before being heated in the oven. After the circuit built and the transistor heated in the oven, the measurement of the drain current, I_D obtained will be recorded. This process is repeated for the other transistor. The drain current, I_D that has been recorded is then used to calculate the value of the threshold voltage, V_{TH} of the transistor with every increment of the temperature. Since the experiment does not obtain the drain current of the transistor, the measurement of voltage and resistance for each component in the circuit were taken and gathered in the tables. The circuit was successfully built but the drain current value was not being able to obtain.

ABSTRAK

Kajian ini merupakan satu analisis kegagalan transistor (MOSFET) dimana pemerhatian nilai voltan ambang, VTH, terhadap peningkatan suhu pada transistor dibuat. Dalam kajian ini, transistor yang digunakan adalah MPF 990 iaitu sebuah transistor jenis MOSFET perluasan saluran-n. Transistor-transistor yang ingin digunakan dalam eksperimen diuji terlebih dahulu untuk menentukan bahawa ia berada dalam keadaan yang baik sebelum ianya dipanaskan di dalam ketuhar. Selepas litar telah dibina dan kemudian pemanasan dilakukan terhadap transistor tersebut, nilai arus salir, I_D diambil dan direkodkan. Proses ini diulang untuk transistor yang berikutnya. Nilai voltan ambang, V_{TH} dikira dengan menggunakan nilai arus salir, I_D yang telah dipanaskan pada setiap peningkatan suhu. Oleh kerana eksperimen dijalankan tidak mendapat nilai arus salir yang sepatutnya, maka nilai voltan dan rintangan pada setiap komponen pada litar dijadualkan. Litar telah berjaya dibina akan tetapi transistor tidak memberikan nilai arus salir yang sepatutnya.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

V_{TH} Threshold Voltage, in Volts, V

V_{GS} Gate-Source Voltage, in Volts, V

V_{DS} Drain-Source Voltage, in Volts, V

I_D Drain Current, in Amperes, A

K Transistor Constant

V_P Pinch-off Voltage in Volts, V

I_S Source Current, in Amperes, A

R_{DS} Drain-Source Resistant, in Ohms, Ω

T Temperature, in Celcius, °C

Si Silicon

SiO_2 Silicon Dioxide

CHAPTER 1

PREFACE

1.1 INTRODUCTION

In this era of superior technology, today's world mostly using high technology equipments to make the standard of living more adequate and uncomplicated or in other words, make life simpler. By achieving this, the latest electronic components or devices are needed to match the engineering desires. This means that it is important to avoid any faulty devices from occurrence which it may leads to circumstances. Thus, device failure analysis is prominently needed in ensuring the devices that created will work as it is intended and also to be more reliable.

This project is focused on Field-Effect Transistor (FET) failure analysis. It intends to determine the cause and provide reason and suggestion for the identified failure from the temperature exposure. An analysis of the FET failure will further improve our understanding on the component's behavior and characteristics, particularly its performance and limitations. The information congregated from this analysis will significantly benefit manufacturers of such electronic components in terms of enhancing

the performance, capabilities and also the longevity of these components. This would convert into advanced and better quality products for the devices. Throughout this project, the enhancement-mode n-channel Metal-oxide-semiconductor-field-effect transistor (E-MOSFET) will be used.

1.2 PURPOSE OF STUDY

The purpose of this study is to find out the effects of temperature on the enhancement-mode n-channel MOSFET.

1.3 OBJECTIVES OF THE STUDY

The objectives of this study are as follows:

1. To build a circuit that is involving the electronic components such as the enhancement-mode n-channel MOSFET, the main component to be test.
2. To conduct test on the enhancement-mode n-channel MOSFET when it is expose to various degree of temperature.
3. To observe the changes of the value of the threshold voltage, V_{TH} when it is expose to various degree of temperature.

1.4 RESEARCH SCOPE

This research will be done at the Electronic Physics Postgraduate Lab of the School of Science and Technology in University Malaysia Sabah. The scope of this research involves the measurement of the drain current, I_D, generated when the temperature are risen until it reach certain level of degree. The value of the drain current, I_D will be recorded by every temperature rise.

1.5 SIGNIFICANCE OF THE STUDY

This study looks for to find out the cause and provide explanation of failure on effect of temperature to the enhancement-mode n-channel MOSFET. As a result of doing this study on this matter, it may help the engineers to better understand its characteristic, capabilities and limitation furthermore hoping that the engineers will be able to design and produce better enhancement-mode-n-channel MOSFET in the future.

1.6 HYPOTHESIS

Every research done is based on learnt theories and these theories are meant as guides in the task of a scientific experiment. Hypothesis is an assumption or expectation of the results before the research or experiment is done.

For this research, the hypothesis is that when the E-MOSFET heated with a range of temperature it will slowly reacts and effecting the performance of the E-MOSFET whereby in the early stages of heating which mean starting from a low temperature, the E-MOSFET might still can be functioning quite well until it reached on the stages where the temperature is much higher, causing the E-MOSFET starts to malfunction.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

One of the most important achievements in the history of electronics was the invention of the transistor by John Bardeen, William Shockley and Walter Brattain in 1948. The transistor which also known as a solid-state or semiconductor were eventually replaced the vacuum tube used in television for instance.

The field-effect transistor (FET) is a type of transistor that relies on an electric field to control the shape and for this reason the conductivity of a 'channel' in a semiconductor material. The concept of the field effect transistor predates the bipolar junction transistor (BJT), though FETs were implemented after BJTs due to the limitations of semiconductor materials and relative effortlessness of manufacturing BJTs compared to FETs at the time. More recently, however, FETs have surpassed BJTs in ease of fabrication and low cost, and currently most electronic circuits use FETs as the fundamental circuit elements. Nowadays, FETs are normally used electronic components in a large number type of devices and electronics appliances.

2.2 FIELD-EFFECT TRANSISTOR (FET)

Field-effect transistor (FET) is similar to bipolar transistor but there are a few differences. FET only has 1 type of charge carrier that is either electron or hole. Besides that, FET has 2 channels that are *n* channel FET and *p* channel FET. Moreover, FET has 3 terminals as shown below (Figure 2.1).

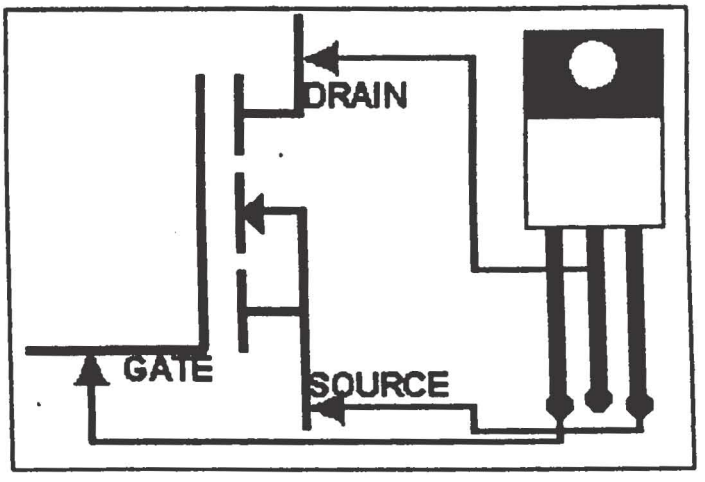


Figure 2.1 The FET

The electron flow from the source terminal to the drain terminal can be controlled by an electric field (hence field effect) set up inside the device by a suitable electric potential applied to the gate terminal. In the input circuit, the gate and channel act like two plates of capacitor. A charge of one polarity on the gate induces an equal and opposite charge in the channel. As a result, the conductivity of the channel can be

increased or decreased by the gate voltage. With an *n* channel, positive voltage at the gate induces negative charges in the channel to allow more electron flow from source to drain (Halliday *et al.*, 2001).

There are many types of transistor that are available now. But there are 2 types of FET that are discuss in this study which are the junction field-effect transistor (JFET) and metal-oxide-semiconductor-field-effect transistor (MOSFET).

2.2.1 Junction Field-Effect Transistor (JFET)

As mention in the Introduction, the junction field effect transistor (JFET) was first proposed and analyzed by William Shockley in 1952. A cross section of the basic device structure is shown in Figure 2.2. In the JFET the application of a gate voltage varies the *pn*-junction depletion widths and the associated electric field in the direction normal to the semiconductor surface. Changes in the depletion widths, in turn, modulate the conductance between the ohmic source and drain contacts.

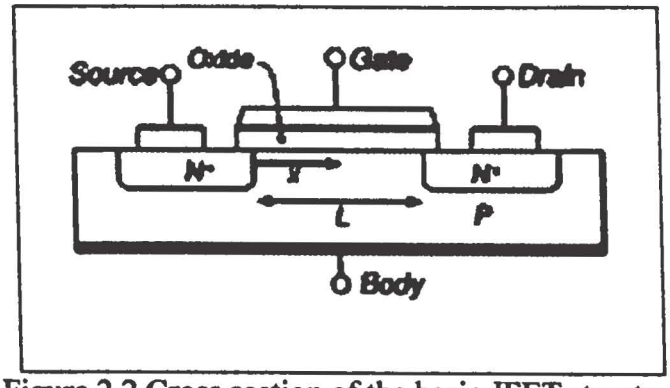


Figure 2.2 Cross section of the basic JFET structure

The JFET was initially named the unipolar transistor to differentiate it from the bipolar junction transistor and to emphasize that only one type of carrier was involved in the operation of the new device. Specifically, for the structure in Figure 2.2, normal operation of the transistor can be described totally in terms of the electrons flowing in the *n* region from the source to the drain. The source (S) terminal gets its name from the fact that the carrier contributing to the current move from the external circuit into the semiconductor at this electrode. The carriers leave the semiconductor, or are "drained" from the semiconductor, at the drain (D) electrode. The gate is so named because of its control or getting action. The modern version of the JFET although somewhat different in physical appearance, is functionally equivalent to the original Shockley structure (Pierret, 1996).

As electrons flow from the source to the drain, they must pass through the narrow channel between the two depletion layers. The more negative the gate voltage is, the tighter the channel becomes (Malvino, 1989). Therefore, the gate voltage can control the current through the channel. The current between the source and the drain is getting smaller as the gate voltage is more negative. More or less all the free electrons passing through the channel flow to the drain. Because of this,

$I_D = I_S$

Where Id is the current through the drain and I_S is the current through the source.

To analyze a JFET, these formulae apply:

$V_P = -V_{GS(off)}$

$R_{DS} = V_P / I_{DSS}$

$K = (1 - V_{GS} / V_{GS(off)})^2$

$I_D = K I_{DSS}$

2.2.2 Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is by far the most common field-effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material, and is accordingly called an N-channel MOSFET or a P-channel MOSFET (also commonly *n*MOSFET, *p*MOSFET).

Placing an insulating layer between the gate and the channel allows for a wider range of control (gate) voltages and further decreases the gate current (and thus increases the device input resistance). The insulator is typically made of an oxide (such as silicon dioxide, SiO_2), This type of device is called a metal-oxide-semiconductor FET (MOSFET) or insulated-gate FET (IGFET). The substrate is often connected to the source internally. The insulated gate is on the opposite side of the channel from the substrate. The bias voltage on the gate terminal either attracts or repels the majority carriers of the substrate across the PN junction with the channel. This narrows (depletes) or widens (enhances) the channel, respectively, as V_{GS} changes polarity. For N-channel MOSFETs, positive gate voltages with respect to the substrate and the source ($V_{GS} > 0$)

repel holes from the channel into the substrate, thereby widening the channel and decreasing channel resistance. Conversely, $V_{GS} < 0$ causes holes to be attracted from the substrate, narrowing the channel and increasing the channel resistance. Once again, the polarities discussed in this example are reversed for P-channel devices. The common short form for an N-channel MOSFET is *NMOS*, and for a P-channel MOSFET, *PMOS*.

2.2.3 The Depletion-Mode Metal-Oxide Semiconductor Field-Effect Transistor (D-MOSFET) and the Enhancement-Mode Metal-Oxide Semiconductor Transistor (E-MOSFET)

The two types of MOSFETs are the depletion type and the enhancement type, and each has *n/p* – channel type. The depletion type is normally on, and operates as a JFET (refer to Figure 2.3).The enhancement type is normally off, which means that the drain to source current increases as the voltage at the gate increases. No current flows when no voltage is supplied at the gate (refer to Figure 2.4).

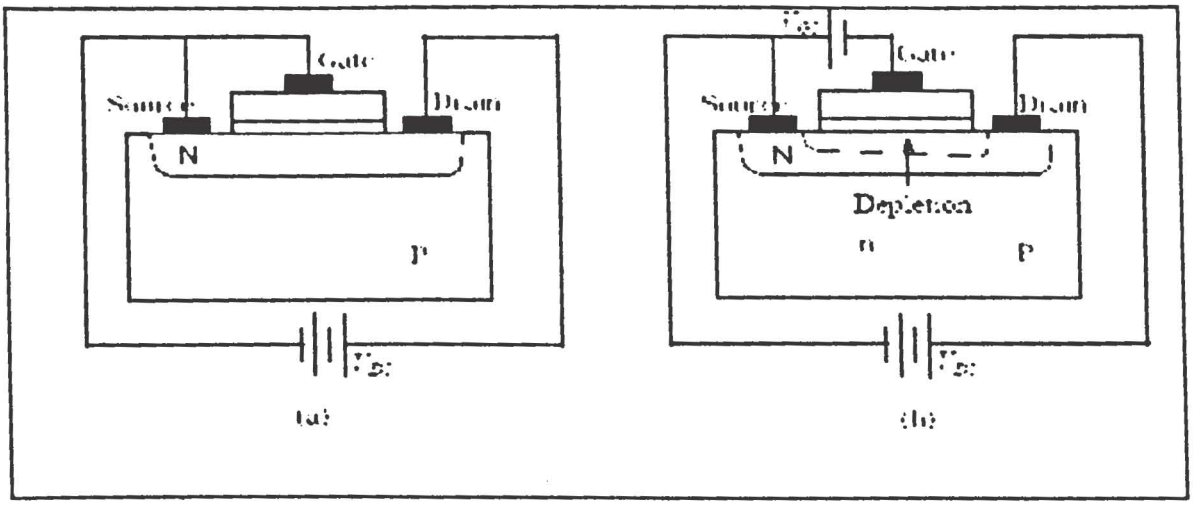


Figure 2.3 The Structure of a Depletion Type MOSFET and its Operation

(a) When V_{GS} (Gate-source voltage) is not supplied

(b) When V_{GS} (Gate-source voltage) is supplied

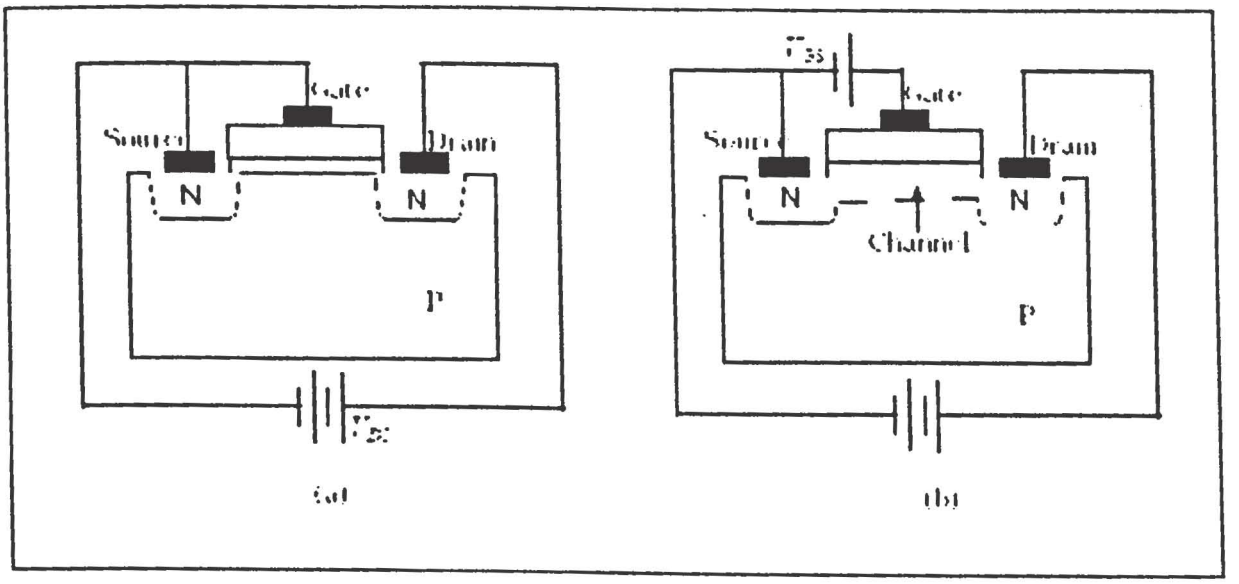


Figure 2.4 The Structure of an Enhancement Type MOSFET and its Operation

(a) When V_{GS} (Gate-source voltage) is not supplied

(b) When V_{GS} (Gate-source voltage) is supplied

a. The Depletion-Mode Metal-Oxide Semiconductor Field-Effect Transistor (D-MOSFET)

The depletion-mode MOSFET structure consists with silicon in which it can be a *p*-type or *n*-type the channel; it is still mostly silicon. Then, the silicon dioxide is simply glass, which is a good insulator. Thus it can form a thin layer of silicon dioxide along one surface of the channel, and then lay a metal gate region down over the glass. The result is shown in the Figure 2.5.

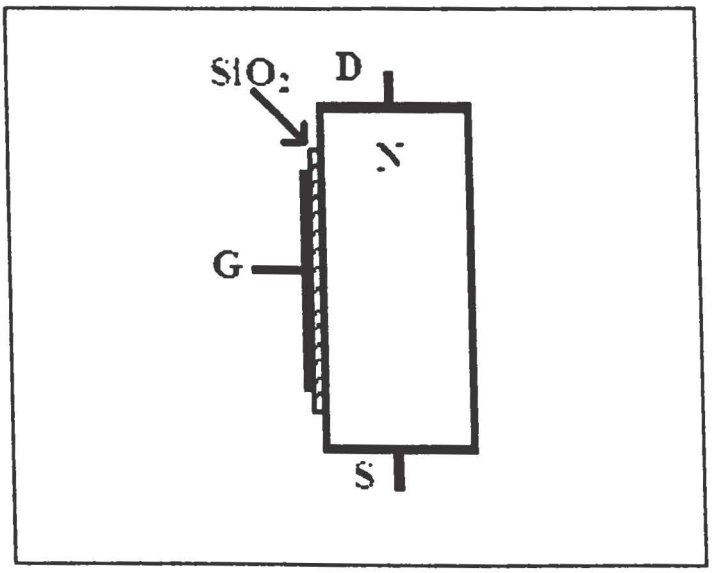


Figure 2.5 The depletion-mode MOSFET structure

This device is sometimes known as an insulated-gate field effect transistor, or IGFET. More commonly, noting the construction of the gate, it is called a metal-oxide-semiconductor *FET*, or MOSFET.

REFERENCES:

Albert Paul Malvino. 1989. *Electronics Principles*.Mcgraw-Hill.

Burhanuddin Yeop Majlis. 2000. *Teknologi Fabrikasi Litar Bersepadu*. Penerbit Universiti Kebangsaan Malaysia : Bangi.

C. Giret, D. Bru, D. Faure, C. Ali, M. Razani, D. Gobled. 2002. Electrical characteristics measurement of transistors by 4 tips-0.2 micron probing technique in Semiconductor Failure Analysis. *Microelectronics Reliability* 42

David Halliday, Robert Resnick and Jearl Walker. 2001. *Fundamentals in Physic*, 5th Edition. John Wiley and Sons, Inc.

Fleeman, S.R. 1990. *Electronic Devices; Discrete and Integrated*. Prentice-Hall, New Jersey.

John T.L. Thong. 1993. *Microdevices: Physics and Fabrication Technologies*. Plenum Press. New York.

Kwok K. Ng. 1995. *Complete Guide to Semiconductor Devices*. McGraw-Hill Series in Electrical and Computer Engineering.

Malik, N.R. 1995. *Electronic Circuits*. Prentice Hall, New Jersey.

Robert F. Pierret.1996. *Semiconductor Device Fundamentals*. Addison-Wesley Publishing Company, Inc.

Thomas L. Floyd. 1996. *Electronic Devices*, 4th Edition. Prentice Hall, USA.