

Investigation of incorporating dielectric pocket (DP) on Vertical Strained-SiGe Impact Ionization MOSFET (VESIMOS-DP)

Abstract

The Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET with Dielectric Pocket (VESIMOS-DP) has been successfully developed and analyzed in this paper. Due to the DP layer, improve stability of threshold voltage, V_T was found for VESIMOS-DP device of various DP size ranging from 20nm to 80nm. The stability is due to the reducing charge sharing effects between source and drain region. However, the presence of DP layer has introduced another potential barrier in addition to $\delta p+$ triangular potential barrier. Thus, increased amount of gate source voltage for lowering both barriers and allows the electron to move from source to drain. Accordingly, slight different and consistency of VESIMOS-DP sub-threshold value as compared to VESIMOS has revealed to give advantages for incorporating DP layer near the drain end. Moreover, the DP layer has suppressed the parasitic bipolar transistor effect with higher breakdown voltage as compared to without DP layer.