Comparison analysis on scaling the vertical and lateral NMOSFET in nanometer regime

Abstract

Conventional lateral and vertical n-channel MOS transistors with channel length in the range of 100 nm to 50 nm have been systematically investigated by means of device simulation. The comparison analysis includes critical parameters that govern device performance. Threshold voltage V-T roll-off, leakage current I-off drain saturation current I-Dsat and subthreshold swing S were analyze and compared between the device. Due to double gate (DG) structure over the side of silicon pillar a better electrostatics potential control of channel is obtained in vertical device shown by, an analysis on V-T roll-off. A two decade higher of I-off in planar device is observed with L-g = 50 nm. A factor of three times larger I-Dsat is observed for vertical MOSFETs compared to planar device. The sub-threshold swing S remains almost the same when the L-g larger than 80 nm. It increased rapidly when the L-g is scaled down to 50 nm due to the short channel effect SCE. However, the vertical device has a steady increase whereas the planar device has suffered immediate enhance of SCE. The analysis results confirmed that vertical MOSFET with double-gate structure is a potential solution to overcome SCE when scaled the channel length to 50 nm and beyond.