**Bias-Induced threshold voltage shifts in organic thin-film transistors by soluble fullerene layers on gate dielectric**


## Abstract

An investigation of threshold voltage shifts in organic thin-film transistors (TFTs) based on pentacene with an additional soluble fullerene derivatives of [6,6]-phenyl C(61)-butyric acid methyl ester (PCBM) on gate dielectric. With an additional soluble fullerene layer, the threshold voltage (V(th)) is optimized from -3: 9 to -1:1 V without affect the mode operation of the devices, while retaining the carrier mobility (0.02-0.03 cm(2) V(-1) s(-1)) and on/off current ratio (similar to 10(4)). Furthermore, the existence of PCBM agglomerates as electron acceptor-like traps resulted in a shift of Vth in the positive and reversible directions depending on the magnitude of gate bias (V(bias)) as well as duration of time bias (T(bias)). The device operation changed into normally-on (depletion-accumulation) mode upon positive Vbias as the duration of Tbias was increased, which attributes to the formation of a conductive layer at the pentacene-fullerene interface. Moreover, the recovery of Vth was further enhanced by a high negative V(bias) for a short duration. In addition, the mobility was minimally affected by both Vbias conditions. (C) 2011 The Japan Society of Applied Physics