EMERGING NANOELECTRONICS DEVICE DESIGN EXPLORATION INCORPORATING VERTICAL IMPACT-IONIZATION MOSFET AND STRAINED (SiGe) TECHNOLOGY

DR ISMAIL SAAD

FINAL REPORT OF EXPLORATORY RESEARCH GRANT SCHEME (ERGS0002-TK-1/2011)

AUGUST 2011 - JULY 2013

SCHOOL OF ENGINEERING AND INFORMATION TECHNOLOGY

UNIVERSITI MALAYSIA SABAH

SYOPSIS

Miniaturization of semiconductor devices beyond sub-100nm has commenced several problems for further scaling. Low subthreshold voltage, reduced carrier mobility, and increased leakage currents were identified to be the paramount issues that leads to high power consumption and heating. The Impact Ionization MOSFET (IMOS) device has evolved to attract increasing attention for its ability to overcome these problems. The IMOS device works on the principle of avalanche breakdown mechanism that gives very good subthreshold slopes of 20mV/decade, but at high supply voltage. Hence, to bring down the supply voltage as well as to obtain low threshold voltage and subthreshold voltage, the Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) has been successfully developed in this study. VESIMOS device integrates vertical structure concept of IMOS and strained SiGe technology. The VESIMOS has been designed and simulated using Silvaco Technology Computer Aided Design (TCAD) tools for both device process (ATHENA) and characterization (ATLAS) respectively. The transfer characteristics of VESIMOS showed an inverse proportionality of supply voltage and subthreshold voltage due to lower breakdown strength of Ge content. However, the subthreshold voltage is in direct proportion to the leakage current. The subthreshold voltage, S=10mV/dec was obtained at threshold voltage, V_{TH}=0.9V, with supply voltage, V_{DS}=1.75V. This V_{TH} was found to be 40% lower than the Si-vertical IMOS device's V_{TH}. The output characteristics of VESIMOS found that the device goes into saturation for supply voltage more than 2.5V, attributed to the presence of Germanium (Ge) that has high and symmetric impact ionization rates. In addition, VESIMOS electron mobility was found to be improved by 40% compared to Si-vertical IMOS, due to the presence of the compressive strain. Consequently, it is also revealed that an increase in strain will also increase mobility and reduce further the threshold voltage. However, the increase in strain layer thickness (T_{SiGe}), resulted in an increase of threshold voltage and lowered the mobility. This is due to the strain relaxation in the SiGe layer. In addition, it is also found that at high source-drain doping concentration (S/D=$2x10^{18}/cm^3$), the threshold voltage dropped to 0.88V, with supply voltage of 1.75V. This is due to high electric field effect in the channel at high doping concentration, which is contrary to the doping effects of conventional MOSFET.

SINOPSIS

Pengecilan saiz peranti-peranti semikonduktor melebihi sub-100nm telah mewujudkan beberapa masalah bagi meneruskan pengskalaan. Sub-ambang rendah, penyusutan mobiliti pembawa dan peningkatan arus bocoran adalah yang dikenalpasti sebagai penyebab utama berlakunya penggunaan kuasa yang tinggi dan pemanasan. Peranti Impact Ionization MOSFET (IMOS) telah dibangunkan dan mendapat perhatian disebabkan keupayaannya bagi menghadapi permasalahan tersebut. Peranti IMOS beroperasi dengan berasaskan prinsip mekanisma kejatuhan 'avalanche' yang membolehkannya mempunyai kecerunan sum-ambang yang sangat baik iaitu 20mV/decade tetapi pada sumber voltan yang tinggi. Maka, bagi menurunkan sumber voltan dan juga mendapatkan voltan ambang dan kecerunan sub-ambang yang rendah, Vertical Strained Silicon-Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) telah berjaya di bangunkan dalam kajian ini. Peranti VESIMOS menggabungkan konsep stuktur menegak IMOS dan teknologi terikan SiGe. VESIMOS telah direkabentuk dan disimulasikan menggunakan peralatan Rekabentuk Berasaskan Teknologi Komputer (TCAD) Silvaco untuk kedua-dua proses (ATHENA) dan pencirian peranti (ATLAS). Ciri pemindahan VESIMOS menunjukkan perkadaran songsang antara sumber voltan dan voltan sub-ambang disebabkan oleh kekuatan kejatuhan yang rendah bagi kandungan Germanium (Ge). Akan tetapi, voltan sub-ambang adalah berkadar terus dengan arus bocoran. Voltan sub-ambang, S=10mV/dec telah diperolehi pada voltan ambang, V_{TH}=0.9V dengan sumber voltan, V_{DS}=1.75V. Nilai V_{TH} ini didapati 40% lebih rendah berbanding V_{TH} bagi peranti Si-vertical IMOS. Ciri keluaran VESIMOS mendapati bahawa peranti akan berada di tahap tepu bagi sumber voltan melebihi 2.5V disebabkan oleh kewujudan Ge yang mempunyai kadar kesan ionisasi tinggi dan simetri. Tambahan lagi, mobiliti elektron VESIMOS telah dapat ditingkatkan sebanyak 40% berbanding Si-vertical IMOS disebabkan oleh kehadiran terikan mampatan. Seterusnya, dapat juga didedahkan bahawa peningkatan terikan akan juga meningkatan mobiliti dan menurunkan voltan ambang. Akan tetapi, peningkatan ketebalan lapisan terikan (T_{SiGe}) akan menghasilkan peningkatan voltan ambang dan menyusutkan mobiliti. Ini adalah disebabkan oleh kelonggaran terikan di lapisan SiGe. Sebagai tambahan, adalah juga didapati bahawa pada kepekatan doping punca-salir (S/D=2x10^{18}/cm^3) voltan ambang akan menyusut ke V_{TH}=0.88V dengan sumber voltan, V_{DS}=1.75V. Ini adalah kerana kesan medan elektrik yang tinggi dalam saluran pada kepekatan doping yang tinggi dimana kesan ini adalah bertentangan dengan kesan doping bagi MOSFET konvensional.