High-k gate dielectric nano-FET leakage current analysis

ABSTRACT

This paper reveals the use of high-k dielectric material to mitigate the subthreshold leakage current. The feature size of conventional MOSFET using SiO_2 has approached their physical limits where the oxide thickness should not reach below 2nm due to high leakage current and the tunnelling increase drastically. Therefore, it is difficult to scale down the size of the MOSFET meanwhile improve its performance. Instead of reducing the size of the transistor, it can make the changes to the parameter, such as the channel length, oxide thickness, and channel width. However, these may affect the performance of the device. Hence, the replacement of SiO_2 with other high-k dielectric material has been analyzed. The material used in the analysis including SiO_2, Al_2O_3, HfO_2, Ta_2O_5, and La_2O_3. The characteristic of subthreshold leakage current was tested through simulation using MATLAB. La_2O_3 as dielectric material shows a good refinement on mitigating the subthreshold leakage current by 87% compared to SiO_2.