DESIGN AND SIMULATION OF VERTICAL STRAINED SiGe IMPACT IONIZATION MOSFET (VESIMOS)

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Abstract

DESIGN AND SIMULATION OF VERTICAL STRAINED SiGe IMPACT IONIZATION MOSFET (VESIMOS)

Miniaturization of semiconductor devices beyond sub-100nm has commenced several problems for further scaling. Low subthreshold voltage, reduced carrier mobility, and increased leakage currents were identified to be the paramount issues that leads to high power consumption and heating. The Impact Ionization MOSFET (IMOS) device has evolved to attract increasing attention for its ability to overcome these problems. The IMOS device works on the principle of avalanche breakdown mechanism that gives very good subthreshold slopes of 20mV/decade, but at high supply voltage. Hence, to bring down the supply voltage as well as to obtain low threshold voltage and subthreshold voltage, the Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) has been successfully developed in this study. VESIMOS device integrates vertical structure concept of IMOS and strained SiGe technology. The VESIMOS has been designed and simulated using Silvaco Technology Computer Aided Design (TCAD) tools for both device process (ATHENA) and characterization (ATLAS) respectively. The transfer characteristics of VESIMOS showed an inverse proportionality of supply voltage and subthreshold voltage due to lower breakdown strength of Ge content. However, the subthreshold voltage is in direct proportion to the leakage current. The subthreshold voltage, S=10mV/dec was obtained at threshold voltage, V_{TH}=0.9V, with supply voltage, V_{DS}=1.75V. This V_{TH} was found to be 40% lower than the Si-vertical IMOS device's V_{TH}. The output characteristics of VESIMOS found that the device goes into saturation for supply voltage more than 2.5V, attributed to the presence of Germanium (Ge) that has high and symmetric impact ionization rates. In addition, VESIMOS electron mobility was found to be improved by 40% compared to Si-vertical IMOS, due to the presence of the compressive strain. Consequently, it is also revealed that an increase in strain will also increase mobility and reduce further the threshold voltage. However, the increase in strain layer thickness (T_{SiGe}), resulted in an increase of threshold voltage and lowered the mobility. This is due to the strain relaxation in the SiGe layer. In addition, it is also

found that at high source-drain doping concentration (S/D=$2x10^{18}/cm^3$), the threshold voltage dropped to 0.88V, with supply voltage of 1.75V. This is due to high electric field effect in the channel at high doping concentration, which is contrary to the doping effects of conventional MOSFET.

Abstrak

Pengecilan saiz peranti-peranti semikonduktor melebihi sub-100nm telah mewujudkan beberapa masalah bagi meneruskan pengskalaan. Sub-ambang rendah, penyusutan mobiliti pembawa dan peningkatan arus bocoran adalah yang dikenalpasti sebagai penyebab utama berlakunya penggunaan kuasa yang tinggi dan pemanasan. Peranti Impact Ionization MOSFET (IMOS) telah dibangunkan dan mendapat perhatian disebabkan keupayaannya bagi menghadapi permasalahan tersebut. Peranti IMOS beroperasi dengan berasaskan prinsip mekanisma kejatuhan 'avalanche' yang membolehkannya mempunyai kecerunan sum-ambang yang sangat baik iaitu 20mV/decade tetapi pada sumber voltan yang tinggi. Maka, bagi menurunkan sumber voltan dan juga mendapatkan voltan ambang dan kecerunan sub-ambang yang rendah, Vertical Strained Silicon-Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) telah berjaya di bangunkan dalam kajian ini. Peranti VESIMOS menggabungkan konsep stuktur menegak IMOS dan teknologi terikan SiGe. VESIMOS telah direkabentuk dan disimulasikan menggunakan peralatan Rekabentuk Berasaskan Teknologi Komputer (TCAD) Silvaco untuk kedua-dua proses (ATHENA) dan pencirian peranti (ATLAS). Ciri pemindahan VESIMOS menunjukkan perkadaran songsang antara sumber voltan dan voltan sub-ambang disebabkan oleh kekuatan kejatuhan yang rendah bagi kandungan Germanium (Ge). Akan tetapi, voltan sub-ambang adalah berkadar terus dengan arus bocoran. Voltan sub-ambang, S=10mV/dec telah diperolehi pada voltan ambang, V_{TH}=0.9V dengan sumber voltan, V_{DS}=1.75V. Nilai V_{TH} ini didapati 40% lebih rendah berbanding V_{TH} bagi peranti Si-vertical IMOS. Ciri keluaran VESIMOS mendapati bahawa peranti akan berada di tahap tepu bagi sumber voltan melebihi 2.5V disebabkan oleh kewujudan Ge yang mempunyai kadar kesan ionisasi tinggi dan simetri. Tambahan lagi, mobiliti elektron VESIMOS telah dapat ditingkatkan sebanyak 40% berbanding Si-vertical IMOS disebabkan oleh kehadiran terikan mampatan. Seterusnya, dapat juga didedahkan bahawa peningkatan terikan akan juga meningkatan mobiliti dan menurunkan voltan ambang. Akan tetapi, peningkatan ketebalan lapisan terikan (T_{SiGe}) akan menghasilkan peningkatan voltan ambang dan menyusutkan mobiliti. Ini adalah disebabkan oleh kelonggaran terikan di lapisan SiGe. Sebagai tambahan, adalah juga didapati bahawa pada kepekatan doping punca-salir (S/D=2x10^{18}/cm^3) voltan ambang akan menyusut ke

V_{TH}=0.88V dengan sumber voltan, V_{DS}=1.75V. Ini adalah kerana kesan medan elektrik yang tinggi dalam saluran pada kepekatan doping yang tinggi dimana kesan ini adalah bertentangan dengan kesan doping bagi MOSFET konvensional.

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LIST OF ABBREVIATIONS

BTBT	Band-to-band tunnelling
CI-MOS	Complementary I-MOS
EHP	Electron-hole pairs
GOI	Germanium on insulator
II	Impact Ionization
I-MOS	Impact ionization MOSFET
LI-MOS	L-shaped IMOS
PDBFET	Planar doped barrier field effect transistor
RIE	Reactive ion etching
RTP	Rapid thermal processing
SCE	Short channel effects
SEG	Selective epitaxial growth
SiGe	Silicon-Germanium
SIMS	Secondary ion mass spectrometry
SNM	Signal-to-noise margin
SOI	Silicon on insulator
TFET	Tunnel field effect transistor
VESIMOS	Vertical strained SiGe IMOS
VWF	Virtual wafer fabrication

LIST OF NOTATIONS

$\vec{E}$	Electric field
$\vec{J}_n$	Electron current density
$\vec{J}_p$	Hole current density
ϕ_B	Barrier height at the metal-semiconductor interface
μ_n	Electron mobility
μ_p	Hole mobility
D_n	Electron diffusivity
D_p	Hole diffusivity
E_G	Bandgap energy
E_i	Ionization energy
G_n	Generation rates for electrons
G_p	Generation rates for holes
kT/q	Boltzmann's constant
L_{ch}	Length of the channel
L_G	Gate Length
L_I	Intrinsic Region Gate Length
q	Magnitude of the charge on an electron
R_n	Recombination rates for electrons

R_p	Recombination rates for holes
T_L	Lattice temperature
T_{Si}	Thickness of the silicon layer
V_{BR}	Breakdown voltage
V_{DS} (or V_D)	Drain voltage
V_G	Gate voltage
V_S	Source voltage
V_{TH} (or V_T)	Threshold voltage
α_n	Ionization coefficients of electrons
α_p	Ionization coefficients of holes
ε	local permittivity
ρ	local space charge density
ψ	Electrostatic potential
ψ_i	intrinsic Fermi potential

CHAPTER 1

INTRODUCTION

1.1 Research Background

Semiconductor device based electronic industry has revolutionized the world with the invention of silicon transistors by William Shockley in 1950's. Since then, silicon has been the heart of semiconductor industry for decades, until now. The reason behind the semiconductor industry thriving for decades can be attributed to the concept of transistor scaling. With scaling or miniaturization, silicon devices have become smaller, faster and better in performance with every new device that has been invented, since its inception.

Due to the realization of Moore's law (Moore G., 1965), today, the miniaturization of silicon devices have provided a path towards denser and faster integration. The transistors manufactured today are 20 times faster and occupy less than 1% of the chip space of those built 20 years ago. It was due to this miniaturization, that it was possible to develop various kinds of miniature devices such as- laptops, mobile phones and hand held Ultrasound devices, which are now a necessity for every human being.

But to what extent can this downsizing of silicon devices can be carried out, is the question posing the semiconductor industry now. As a result of continued miniaturization of silicon devices, beyond sub-100nm, the industry is posing several problems such as- high subthreshold slopes, reduced carrier mobility, increased leakage currents and hence high power consumption and heating, thus questioning the reliability of smaller devices. Therefore, the researchers in this industry are looking for alternative ways to continue producing miniature devices that can perform efficiently. As a result, the semiconductor industry has been successful in scaling the devices up to 45nm till date, and is striving to go beyond 45nm limit.

Impact Ionization MOSFET (I-MOS), is one such attempt to produce better performing devices at a nano-scale level. It uses impact ionization mechanism of carrier injection. Impact Ionization (II) occurs when a carrier is placed in a high electric field, thus acquiring energy. This carrier becomes a hot carrier and when it collides with the lattice, loses its kinetic energy to generate electron-hole pairs (EHP). II leads to avalanche multiplication and eventually avalanche breakdown (Kwok K. Ng, 1995).

I-MOS works on the principle of avalanche breakdown mechanism of p-i-n diodes, induced by impact ionization. The carrier transport mechanism in this device is due to drift, rather than diffusion mechanism. This mechanism provides excellent subthreshold slopes of less than 10-20mV/decade (K. Gopalakrishnan *et.al.,* 2002). But, as I-MOS works on the concept of impact ionization, it requires high operating voltages, which results in hot carrier degradation effects. This leads to poor reliability of the planar I-MOS device, as it results in hot-carrier degradation effects such as, shifts in threshold voltage and subthreshold slopes. Therefore, a novel vertical concept of I-MOS device was developed (Abelein U., *et al.,* 2006). The device structure of vertical I-MOS offers an arbitrary choice of doping between the source and the drain regions. It also works on the principle of impact ionization mechanism of carrier injection. The holes generated due to the impact ionization charge the floating p-body, which results in dynamic reduction of threshold voltage and a fast rising drain current. Moreover, the channel is formed in the bulk- Si region and is not confined to the Si/SiO2 region. As a result, the device does not suffer from either the threshold voltage shifts or the subthreshold slope shifts. It also provides good subthreshold slopes of <20 mV/decade. To achieve desired device characteristics, relatively high supply voltages are to be provided and hence, high threshold voltages.

The best alternative to reduce the supply voltages is to incorporate strain in the vertical I-MOS device (Dinh T.V., *et al.,* 2009).The VESIMOS (vertical strained SiGe IMOS) device concept was developed with this idea. A thin strained SiGe layer was placed in the channel region towards the drain-side intrinsic region of the vertical I-MOS. A compressive biaxial strain is developed when the SiGe layer is