Design and simulation analysis of vertical double-gate MOSFET (VDGM) structure for nano-device application

Abstract

Design and simulation analysis of vertical MOSFET structure with double gate structure on each side of insulating pillar for nanodevice applications is presented. The body doping effect on vertical channel for channel length, L g = 50nm and analyzing its effect towards such small devices was successfully performed. The analysis continued with the comparative investigation of device performance with conventional planar MOSFET as scaling L g down to 50nm. The final part evaluates the innovative design of incorporating dielectric pocket (DP) on top of vertical MOSFET turret with comprehensive device performance analysis as compared to standard vertical MOSFET in nanoscale realm. An optimized body doping for enhanced performance of vertical MOSFET was revealed. The vicinity of DP near the drain end is found to reduce the charge sharing effects between source and drain that gives better gate control of the depletion region for short channel effect (SCE) suppression in nanodevice structure.