THE SIMULATION OF ELECTRICAL *I-V* CHARACTERISTICS OF METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISOR (MOSFET) BY USING PISCES IIB 9009

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IJAZAH: B-Sc

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I hereby declare that this dissertation is the result of my work, except the quotations and summaries, each of which the sources has been mentioned.

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ABSTRACT

In this study, PISCES IIB 9009 device simulator is used to obtain drain current of MOSFET. There are four factors to discuss and comparison the *IV* characteristics of MOSFET. The four factors are gate thickness, doping concentration, width in y axis, and different material with gallium arsenide. These four factors are changes its value and the simulation results are plot. The POSTMINI software is used to verify the structure MOSFET before run the solve parts in simulator. To solve the threshold voltage of MOSFET, the gate voltage is increased from 0V to 3.0V and the drain current is set to 0.1V, the data drain current is collected from the PISCES simulator output. To solve the drain characteristics of MOSFET, the drain voltage is increased from 0V to 3.0V and the gate voltage is set to constant value, the data drain current is then collected from the PISCES simulator. The graph I_d against V_g and graph I_d against V_d were plotted to obtain the *IV* characteristics of MOSFET. The factors that influence the threshold voltage and saturation current were being studied. The structure of MOSFET in this study is n-channel enhancement MOSFET with the length is 3.0 μm and width is 2.0 μm. Due to the small size device, the drain current is small, which is around 40 μA. The threshold voltage is around 0.5V to 2.0V and it is suitable to use as switch in the electronics. The results show gallium arsenide having the higher saturation current than silicon.

ABSTRAK

Dalam kajian ini, perisian PISCES IIB 9009 telah digunakan untuk mendapatkan arus saliran bagi MOSFET. Ciri-ciri arus dan voltan bagi MOSFET akan dibincang dan perbandingan dengan Empat faktor yang berlainan akan diadakan. Empat faktor yang dijangka akan memberi kesan kepada arus dan voltan ialah ketebalan get, ketumpatan dopant, lebar y axis, dan bahan yang berbeza, gallium arsenide. Nilai-nilai bagi empat factor tersebut akan berubah dan membincangkan hasilnya dengan poltkan graft. Perisian POSTMINI digunakan untuk menentukan struktur MOSFET sebelum membuat simulasi terhadap penyelesaian. Untuk mendapatkan penyelasaian terhadap voltan ambang, voltan get dinaikan dari 0V ke 3.0V dan voltan saliran ditetapkan kepada 0.1V, data bagi arus saliran dikumpul dari perisian PISCES. Untuk mendapatkan penyelesaian terhadap ciri-ciri arus, voltan saliran akan dinaikkan dari 0V ke 3.0V, voltan get ditetapkan kepada nilai konstant dan data bagi arus saliran dikumpul dari perisian PISCES. Graft I_d melawan V_g dan graft I_d melawan V_d dipoltkan untuk mendapatkan ciri-ciri arus dan voltan bagi MOSFET. Factor-faktor yang memberi kesan kepada voltan ambang dan arus ketepuan bagi MOSFET akan dikaji. Struktur MOSFET yang akan disimulasikan ialah NMOSFET, panjang dan lebar bagi MOSFET ialah 3.0 µm dan 2.0 µm masing-masing. Oleh kerana saiz MOSFET sangat kecil, arus saliran asalah kecil, iaitu kira-kira 40 µA. Voltan ambang ialah diantara 0.5V hingga 2.0V, sesuai untuk berfungsi sebagai suis dalam litar elektrik. Hasil juga menggambarkan arus ketepuan bagi gallium arsenide adalah juah berbeza dengan silikon.

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C_{OX} gate oxide capacitance per unit area

I current
I_{DS} drain to source current
I_D drain current
I_{D1} MOSFET dc drain current
$I_{D,sat}$ drain current in saturation
I_{DSS} drain to source current in saturation

K MOSFET device parameter

L gate length

n_i intrinsic carrier concentration of Silicon
N_d donor concentration
N_a acceptor concentration
N doping concentration

$g_{m,quad}$ small-signal transconductance in quadratic model
$g_{m,sat}$ small-signal transconductance in saturation
g_d small-signal drain conductance
$g_{d,sat}$ small-signal drain conductance in saturation

p minority carrier concentration

Q_{inv} inversion layer charge per unit area
q unit electronic charge, $=1.6\times10^{-9}$ C

r_j depth of the source and drain island in MOSFET

t_{OX} thickness
t_r transit time

v velocity
V voltage
V_D drain voltage
V_G gate voltage
V_{GS} gate to source voltage.
V_T threshold voltage of MOSFET

V_{FB}	flat-band voltage in MOSFET
$V_{GS(th)}$	gate to source threshold voltage.
V_{DS}	drain to source voltage
V_P	pinchoff voltage in MOSFET
ΔV_T	change in the threshold voltage due to the small effect
W	gate width
W_T	depletion width
Z	gate width
Π	pi constant
ε	permittivity
ε_S	permittivity of semiconductor
λ	constant,
μ_n	charge-carrier mobility
μ_e	electron drift mobility in the channel
ϕ_S	semiconductor work function voltage
ϕ_B	metal work function voltage

E-MOS	enhancement metal oxide silicon
D-MOS	depletion metal oxide silicon
IC	integrate circuit
MOSFET	metal oxide semiconductor field effect transistor
MISFET	metal insulated field effect transistor
NMOSFET	n channel metal oxide semiconductor field effect transistor
PMOSFET	p channel metal oxide semiconductor field effect transistor
Si	silicon
SiO_2	silicon dioxide

CHAPTER 1

INTRODUCTION

1.1 History and Background

The metal-oxide-semiconductor field-effect-transistor is known as MOSFET. According to Ng (2002), MOSFET belongs to a general group of device, called IGFET (insulated-gate field-effect-transistor) or MISFET (metal-insulator-semiconductor field-effect-transistor).

Lilienfeld and Heil are purposed a conceptually similar MOSFET structure in 1926 and 1935 respectively. During the late 1940s, experiments are focused on the field-effect device. Unfortunately, MOSFET is not successfully demonstrated until the late 1960. The main technological problem in making MOSFET is the control and reduction of the surface states at the interface between the oxide and the semiconductor.

In 1955, Ross proposed using the field effect on minority carriers in the surface inversion layer, and the Si/SiO_2 system is first proposed in 1960 by Atalla (Ng, 2002). After that, the popularity of MOSFET is rising.

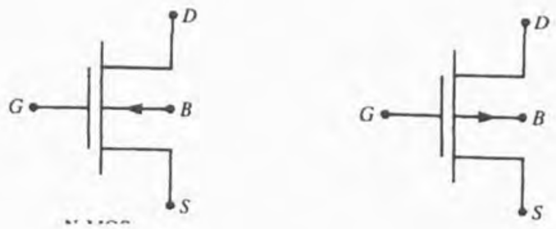
Early MOSFET are dominated by p-channel devices because of the inability to realize enhancement mode for n-channel devices due to positive oxide charges (Ng, 2002). The quality of oxide is improved and n-channel devices provided improved performance due to the higher electron mobility.

By now, most MOSFET are enhancement-mode devices. The MOSFET is the most common transistor found in commercial ICs because of its simplicity, low cost, small size, and low power (Ng, 2002). The stucture of MOSFET always changes to be efficient in sector microelectronics.

1.2 Introduction of MOSFET

The MOSFET is the most common transistor in both digital and analog circuits. There are two types of MOSFET: the depletion-type (D-MOS) and the enhancement-type (E-MOS). D-MOS can be operated in both the depletion mode and the enhancement mode, whereas E-MOS are restricted to operating the enhancement mode (Paynter, 2003).

The MOSFET is composed of a channel of n-type or p-type semiconductor material and accordingly called NMOSFET or PMOSFET. The difference between the circuit diagram of NMOSFET and PMOSFET is indicated by the direction of the arrow (Figure 1.1).



NMOSFET PMOSFET

Figure 1.1 Circuit diagram symbols of NMOSFET and PMOSFET (Mauro, 1989).

The MOSFET devices have four terminals. It is source, drain, gate and substrate. The function of gate in the MOSFET is like the base terminal in the bipolar transistor. It used to control the current flow between the source and drain.

1.3 Purpose of Study

The aim of this research paper is to study the current and voltage characteristics of MOSFET by using the two-dimension device simulator, PISCES IIB.

1.4 Objective

The goal of this research paper is to study the current and voltage characteristics of MOSFET. To achieve the goal, there are two objectives as follow:

1. To simulation a MOSFET device using PISCES IIB.

2. To study the current and voltage characteristics of MOSFET by changes the parameter below:
    a. Gate thickness
    b. Width
    c. Concentration
    d. Material

1.5 Scope

The scope of this research paper is analyzing the current and voltage characteristics of n-channel MOSFET by using two-dimension device simulator, PISCES IIB 9009. The parameter to be study is gate thickness, width, and concentration. After that, the parameter above is analyze with changes the material from silicon to gallium arsenide.

CHAPTER 2

LITERITURE REVIEW

2.1 Structure of NMOSFET

In the structure of NMOSFET, the source and drain is n regions and the body is p region (Figure 2.1). The substrate in NMOSFET is p-type material and the source and drain are n-type material.

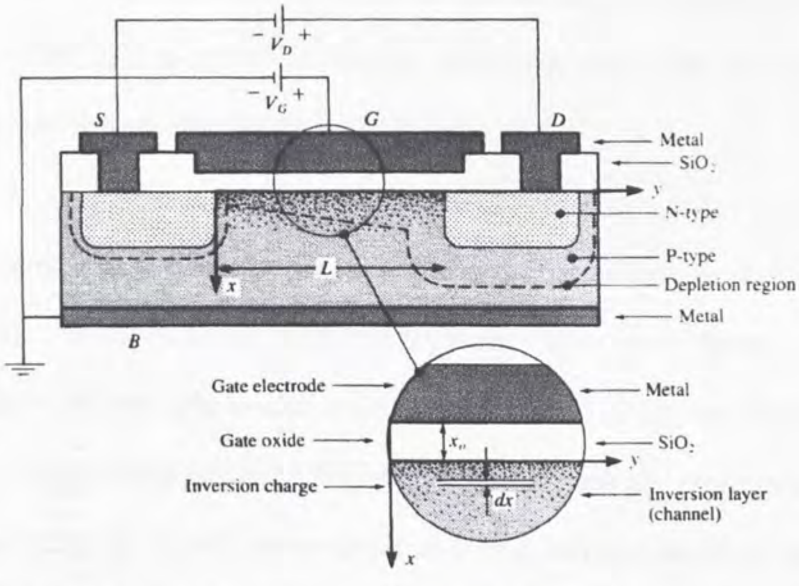


Figure 2.1 Structure of a bias N-channel MOSFET (Mauro, 1989).

Normally, the MOSFET device is symmetrical so that the source and drain can be interchange. The distance between the metallurgical junction is the effective channel length L. The oxide in MOSFET is grown thermally for good interfacial properties.

According to Ng (2002), for a channel length of 0.3 μm, typical parameters are: oxide thickness ≈ 10 nm, substrate doping $\approx 3 \times 10^{17}$ cm^{-3}, and source and drain junction depth ≈ 0.2 μm. Normally, an optimized MOSFET structure has non-uniform substrate doping in the y-direction and has a bell-shape profile.

NMOSFET can be as much as three times faster than equivalent PMOSFET and are often preferred, especially for high-speed applications (Mauro, 1989).

2.1.1 N-Type Material

Silicon crystal is very stable and cannot conduct electricity due to the strong covalent bond. To allow silicon crystal to conduct electricity, must find a way to allow electrons to move from place to place within the crystal.

Arsenic is added into the silicon crystal structure to form the n-type material (Figure 2.2). The silicon atoms bond with the arsenic atom, each sharing one arsenic electron. However, the fifth arsenic electron is not bound to any surrounding silicon atoms. The fifth electron requires a little energy to break free and enter the conduction band. As a result, the crystal has an excess of current-carrying electrons, each with a negative charge. This material is known as n-type silicon.

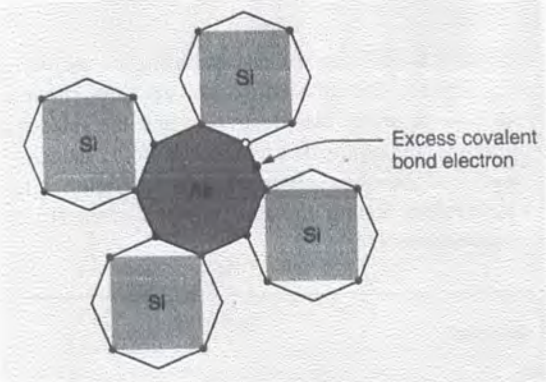


Figure 2.2 N-type material (Paynter, 2003).

Because there are more conduction-band electrons than valence-band holes in the n-type material, the electrons are called majority carriers, and the valence-band holes are called minority carriers (Paynter, 2003). N-type material is a donor-doped material. It is containing more electrons than holes (Pierret, 1996).

The minority carrier concentration can find as (Pokharel & Karki, 2007):

$$p \approx \frac{n_i^{\,2}}{N_d} \tag{2.1}$$

where n_i = intrinsic carrier concentration of Silicon

N_d = donor concentration

2.1.2 P-Type Material

According to Paynter (2003), when intrinsic silicon is doped with a trivalent element, the resulting material is called p-type material. Trivalent element causes the existence of a hole in the covalent bonding structure (Figure 2.3).

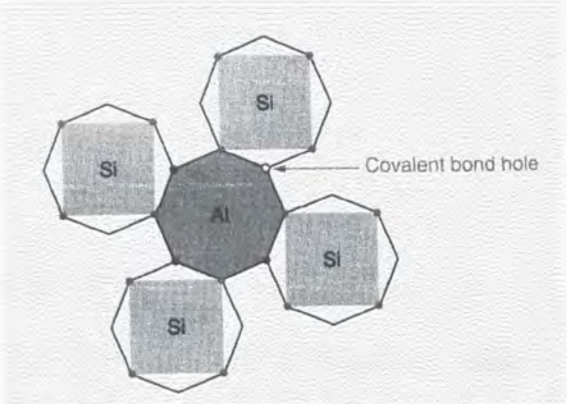


Figure 2.3 P-type material (Paynter, 2003).

The aluminum atom is surrounded by four silicon atoms. There is a gap in the covalent bond caused by the lack of a fourth valence electron in the aluminum atom. It is an excess of holes in the covalent bonds.

There is an empty place where an electron should logically go, and often an electron will try to move into that space to fill it. However, the electron filling the hole had to leave a covalent bond behind to fill this empty space, and therefore leaves another hole behind as it moves. After that, another electron may move into that hole and leaving another hole behind.

Holes appear to move as positive charges through the crystal. Therefore, this type of semiconductor material is called p-type material. P-type material is an acceptor-doped material (Pierret, 1996). It is containing more holes than electrons.

The minority carrier concentration can find as (Pokharel & Karki, 2007):

$$p \approx N_a \tag{2.2}$$

where N_a = acceptor concentration

2.2 Operation of MOSFET

In contrast, the true MOSFET is an enhancement-mode or normally off device (Whitaker, 2000). The device is normally off because no majority-carrier current can flow between the p-n junctions.

According Streetman (1995), when a positive voltage is applied to the gate relative to the substrate, positive charges are in effect deposited on the gate metal. The negative charges are induced in the underlying silicon. The depletion region and thin surface region is formed in the underlying silicon (Figure 2.4). This conducting channel is called the inversion layer. No gate current is required to maintain the inversion layer at the interface since the gate oxide blocks any carrier flow. Then, the applied gate voltage may control the current flows between drain and source.

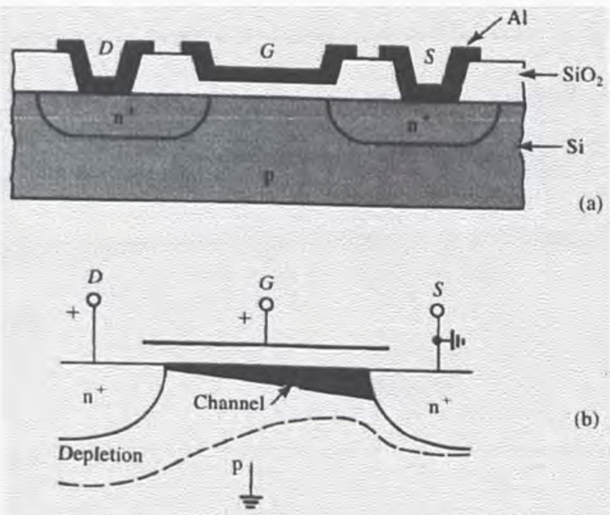


Figure 2.4 Cross section and schematic illustration of MOSFET (Streetman, 1995).

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