

# High luminescence efficient Ga polarity domain GaN realized on Si(111) by MOVPE

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**Abstract**-The stress and defect generation; hence luminescence efficiency of semiconductor materials is correlated. Even severe cracks are formed on the epilayer surface due to stress those impair the photoluminescence property of devices. So the stress effect of GaN epilayer grown on Si(111) is evaluated by different growth approaches and different interlayer's. Epilayer on thinner converted SiC templates is found to increase PL Ex. peak energy with broadening its line width whereas epilayer grown on porously converted GaN layer is found comparatively low PL Ex. peak energy with narrowing its line width. From Raman scattering analysis, it is also observed that the PL Ex. peak is not signifies actual stress level rather its reveals epilayer quality. PL Ex. Peak energy is found to increase with increasing thickness of epilayer grown on converted interlayer on Si substrate.

## I. INTRODUCTION

Direct and higher band gap compound semiconductor materials residual stress and subsequent crack formation on the epilayer surface is detrimental for optoelectronic device fabrication. The residual stress effect of GaN epilayer grown on Si(111) is evaluated by different growth approaches and by using different interlayer's. The investigations of GaN epilayer residual stress for the template of converted interlayer formed by novel nitridation process of very thin GaAs layer on Si(111) and C<sup>+</sup> ion implanted very thin SiC layer formed on Si(111) as well as growth ambient effect are made. Epilayer out of plane lattice strain variation of different growth approach samples grown at 1000°C is mainly due to the interface layer structure and growth methods are revealed. Raman

scattering analysis shows that the epilayer grown on converted interlayer has reduced stress though PL Ex. Peak energy is found to increase with increasing thickness of epilayer grown on converted interlayer on Si substrate. It is also observed that the PL Ex. peak is not signifies actual stress level rather its reveals epilayer quality.

## II. EXPERIMENTAL

In case of performance aspects sapphire is less attractive than Si for laser diode (LDs) and light emitting diode (LEDs) and for the integration of GaN.<sup>1-3</sup> Due to poor thermal conductivity of sapphire, it prevents dissipation of heat for high power and high current operating devices.<sup>4</sup> But for better quality optoelectronic device fabrication, impact of higher residual stress or cracking in the epilayer for GaN epitaxy on Si is a detrimental.<sup>5</sup>

For hetroepitaxy, buffer layer acts as a wetting layer for improvement of epitaxial layer quality. The strain situation for a layer of particular temperature depends on growth techniques and for proper interface layer structure. Porous/intermittent converted layer (CL) is formed from conversion of cleavage GaAs surface into GaN by inter diffusion of N→As as it was done by other group to take advantage of higher electro negativity of N atom.<sup>6</sup> Then h-GaN epitaxy is made on Si by using converted GaAs layer by formation of low temperature GaN coating layer prior to nitridation of GaAs surface. Due to the variation of lattice bond length and atomic raddi of As and N atoms the converted GaN layer is formed defective and porous. Si

interlayer formed by  $C^+$  ion implantation on Si(111) also thought to be defective between crystalline SiC template and Si substrate, as it was found by other group.<sup>7-8</sup> So such interface defects and porous interface layer appears effectively to reduce epilayer residual thermal stress during post growth cooling.<sup>9</sup> It is revealed by comparing to the epilayer grown on Si with direct nitridated GaAs surface and from In-doped non crack GaN sample grown on Si.<sup>10</sup>

### III. RESULT AND DISCUSSION

Due to porous interface realized between GaN epilayer and Si wafer, the thermal stress seems to be reduced significantly during the crystalline epitaxial layer cooling down from 1000°C to room temperature, So from the scanning electron microscopic (SEM) view, the surface morphology is found very smooth and without cracks. The following figure 1, shows the surface morphology for GaN epilayer grown on Si(111) with porous interlayer(a) and with AlN interlayer (b)<sup>11</sup>.

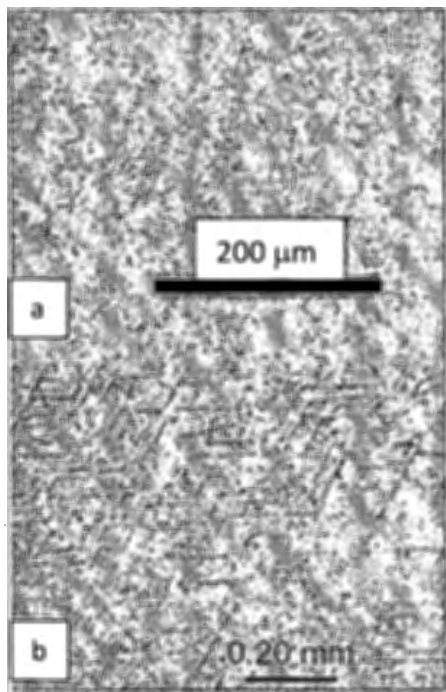


Fig. 1 GaN/Si(111) surface view grown by using porous GaN (a-above) and AlN (b-below) interlayer

h-GaN growth direction is the direction of out of plane lattice constant  $c$ , which usually contracts or dilates for biaxial strain. The thermal stress of GaN layer grown on Si, acts biaxially to make short of its out of plane lattice constant due to cooling down from the growth temperature to room temperature.

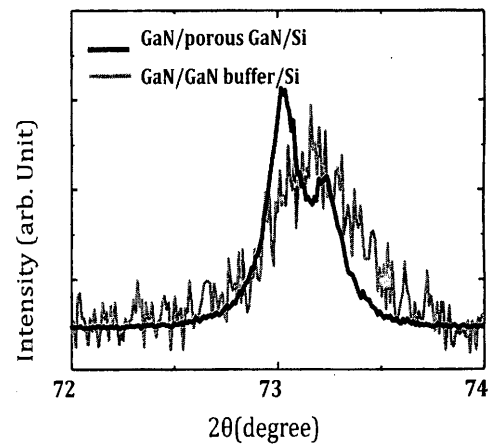


Fig. 3 GaN(004) XRD to observe  $K_{\alpha 1}$  and  $K_{\alpha 2}$  related peak for both growth process

Room temperature XRD comprises the stress of GaN layer due to growth and the thermal stress.<sup>12</sup> Using porous and iso-electronic interlayer we have found to reduce both growth and thermal stress. So out of plane lattice strain is found to be decreased using such interlayer in compare to the epilayer grown on GaN buffer only. The prominent  $K_{\alpha 1}$  and  $K_{\alpha 2}$  related peaks are also found for epilayer grown on porous GaN interlayer whereas no distinguishable such peaks are found for epilayer grown on GaN buffer as shown in figure 2. It seems to be poly type GaN on GaN buffer. Si(111). It may be due to polarity/ polarization effect of interlayer. By calculating the GaN(004) plane scattering result the least lattice strain is found for epilayer grown on porous interlayer.

The below figure 3 shows the PL spectrum of GaN film grown in novel approach on Si(111) using porous GaN interlayer. The extensive near band edge luminescence peak is found for the GaN layer grown on Si(111) using porous

interlayer whereas minimum intensity with comparable defect related yellow band luminescence is found for GaN grown on GaN buffer. Due to reduce stress in the epilayer the defect appears to be reduces, so intense NBE emission intensity with negligible defect related yellow band intensity at room temperature PL measurement is realized.

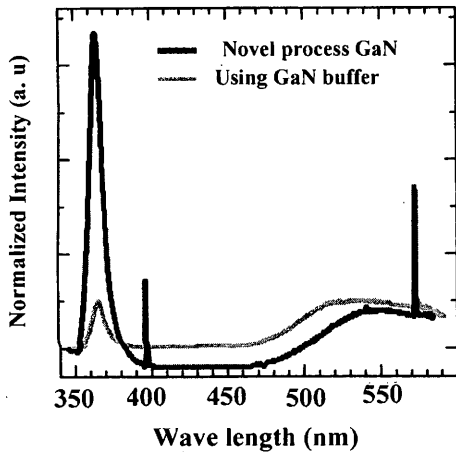


Fig. 4 Room temperature GaN epilayer PL spectrum grown on Si(111)

Following figure 5 shows the PL excitonic peak width variation with interlayer. Using very thin SiC interface layer

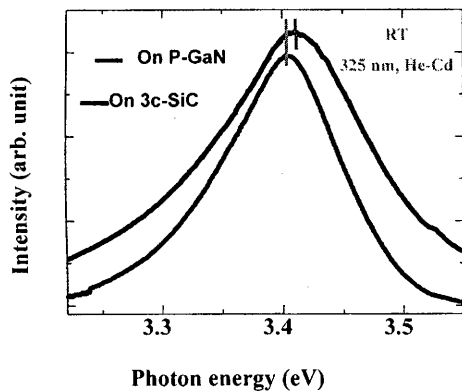


Fig. 5 GaN NBE PL peak grown on Si(111) using porous GaN and converted SiC interlayer

surface of the epilayer not found to be improved rather large inversion domain seems to be related to be broadened the

line width. Epilayer grown with an interlayer on porously converted GaN interlayer, narrow PL line width is found though excitonic peak energy was found little bit lower as compared to epilayer on SiC interlayer. It is not due to stress but may be due to free carrier as it is revealed by Raman scattering analysis. Raman analysis for carrier related  $A_1(LO)$  peak for two different Ex. peak energy films are performed as it is shown in figure 6. It is generally to be

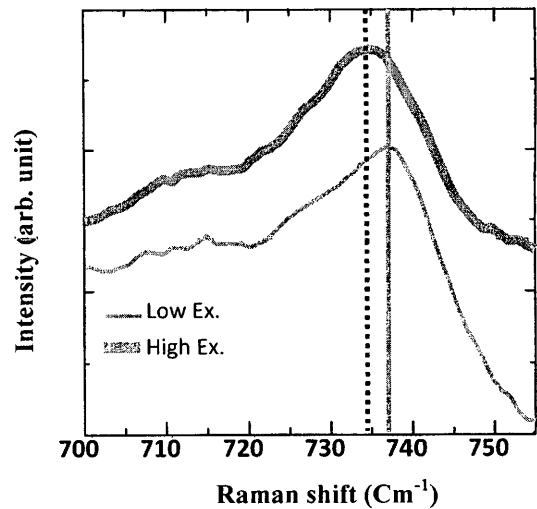


Fig. 6  $A_1(LO)$  peaks of two different epilayer on porous GaN (low Ex.) and on SiC(high Ex.)

known that n-type GaN film carrier or residual impurities have an effect to make variation of near band edge peak energy. Inhomogeneous impurities or local defects leading to the space-charge scattering of carriers and the red shift of the PL line are found. Due to conductive Si substrate, carrier concentration of GaN film by Hall measurement is not realized. Raman spectroscopy has proven to be a useful tool for analyzing the effect of free electron on the lattice dynamics of n-type GaN. When an appreciable carrier concentration is present in polar semiconductor (h-GaN), LO- phonon oscillations of the free carrier may occur<sup>13</sup>. It is also revealed by h-GaN,  $E_2$  (high) phonon frequency observed by Raman scattering analysis as it is shown below. The GaN epilayer grown on Si(111) substrate using porous

interface layer, the epilayer stress is found to share with the defective and porous interface layer during cooling the substrate and due to porosity it seems to be more flexible to reduce stress.<sup>12</sup> So it appears that apart from the Si substrate epilayer achieve relatively improve in quality. The epilayer grown on such iso-electronic interlayer is found to the PL energy level similar to Ga polarity GaN grown on Al<sub>2</sub>O<sub>3</sub>. KOH wet etching also revealed it.

Due to piezoelectric property of h-GaN, E<sub>2</sub> (high) phonon frequency of Raman scattering analysis is highly sensitive to the lattice out of plane lattice constant and its frequency is varied for biaxial strain. GaN epilayer grown heteroepitaxially on Si substrate is not found to increase its E<sub>2</sub> (high) phonon frequency for SiC interlayer. GaN E<sub>2</sub>(high) peak for the epilayers grown on porously converted GaN interlayer and on SiC template is found 565.3 and 565.5 Cm<sup>-1</sup> respectively as shown in figure 7.

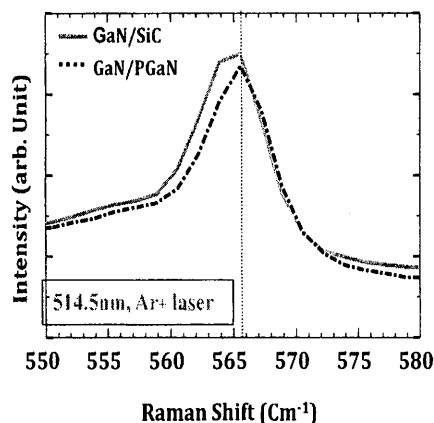


Fig. 7 GaN E<sub>2</sub> (high) phonon frequency on Si(111)

From those results it is observed that the PL Ex. peak is not signifies actual stress level rather its reveals epilayer quality. Epilayer out of plane lattice strain variation of different interlayer approach samples grown at 1000°C is mainly due to the interface layer structure. The GaN epilayer grown on Si(111) substrate using porous interface layer and on SiC interlayer formed by C<sup>+</sup> ion implantation

on Si(111) was found near to stress free level. As per M. Mynbaeva et. al. experiment due to 4.2 cm<sup>-1</sup> of Raman shift of E<sub>2</sub>(high) phonon frequency occurs for 1Gpa of stress incorporation in the epilayer<sup>14</sup>. So the grown epilayer stress level is found minimum as it is revealed by Raman scattering analysis.

#### IV. CONCLUSION

Depending on pre-growth process, the out of plane lattice strain and epilayer residual strain variation is found. The GaN epilayer grown on Si(111) substrate using porous interface layer and on SiC interlayer formed by C<sup>+</sup> ion implantation on Si(111) was found near to stress free level. The epilayer grown on iso-electronic structure interlayer (p-GaN) is found to the PL energy level similar to Ga polarity GaN grown on Al<sub>2</sub>O<sub>3</sub>. It is observed that the PL Ex. peak not signifies actual stress level rather its reveals epilayer quality. Raman scattering analysis is also revealed it.

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